

0300055

(12) United States Patent Fukuda et al.

(10) Patent No.:

US 6,335,883 B1

(45) Date of Patent:

Jan. 1, 2002

(54) MEMORY CONFIGURATION OF A COMPOSITE MEMORY DEVICE

(75) Inventors: Minoru Fukuda, Sanda; Hiroaki

Nakanishi, Kobe; Kunio Matsudaira, Kobe; Masahiro Matsuo, Kobe; Hirohisa Abe, Sanda, all of (JP)

(73) Assignee: Ricoh Company, Ltd., Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this

patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/628,825

(22) Filed: Jul. 31, 2000

Related U.S. Application Data

(62) Division of application No. 09/080,696, filed on May 18, 1998, now Pat. No. 6,115,292.

(30)	Foreign	Application	Priority	Data
------	---------	-------------	-----------------	------

(JP) 9-149975	23, 1997	May
G11C 16/04	Int. Cl.7	(51)
365/185.33; 365/189.04	(52) U.S. Cl	
365/230.00		
Search 365/185.33, 218	Field of	(58) 1
365/230.03, 189.05, 230.06, 189.04	11010 01 0	

(56) References Cited

U.S. PATENT DOCUMENTS

5,245,572 A	• 9/1993	Kosonocky et al 365/189.02
		terada et al 365/218
5,343,434 A	8/1994	Noguchi
5,361,343 A	* 11/1994	Kosonocky et al 395/425
5,469,390 A	11/1995	Sasaki et al.
5 539 688 A	7/1996	Yiu et al.

5,596,530 A 5,630,093 A 5,715,193 A 5,793,676 A 5,818,848 A 5,821,909 A 5,841,696 A	5/1997 • 2/1998 8/1998 10/1998 10/1998	Lin et al. Holzhammer et al. Norman 365/185.02 Bedarida et al. Lin et al. Yiu et al. Chen et al.
6,016,270 A		Thummalapally et al 365/ 185.11

OTHER PUBLICATIONS

STMicroelectronics, "Advanced Architecture Flash Memory—Computers and Peripherals", pp. 1–2, 1999. STMicroelectronics, "32 Mbit (2Mbx16, Dual Bank, Page) Low Voltage Flash Memory", pp. 1–38, Oct., 1999. AMD, "Am29DL800T/Am29DL800B—8 Megabit (1MX8—Bit/512 KX16-Bit) CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory", pp. 1–10, May 1997. Atmel, 4 Megabit 5-volt Flash with 256K E²PROM Memory, AT29C432 Concurrent Flash, pp. 1–11.

* cited by examiner

Primary Examiner—David Nelms
Assistant Examiner—Thong Le
(74) Attorney, Agent, or Firm—Cooper & Dunham LLP

(57) ABSTRACT

The present invention is related to a composite flash memory device comprises a plural sector flash memory array which is divided to plural sector that is a minimum erasing unit of the flash memory device, a flash memory array storing control commands which control a total system of the composite flash memory device and/or the only composite flash memory device in and sharing I/O line of the plural sector flash memory array, the read operation of the flash memory array is enable when the plural sector flash memory array is gained access.

34 Claims, 6 Drawing Sheets

